	L #	Hits	Search Text	DBs	Time Stamp
1	L1	4783582	grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
2	L2	1606143	die or dice or IC or "integrated circuit" or chip or chips	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
3	L3	12329621	contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
4	L4	3235072	encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	138794	(grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
6	L6	366534	"438"/$.ccls. or "257"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
7	L7	31823	((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips)) same (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)	USPAT	2005/01/21 13:46
8	L8	6573	(((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips)) same (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)) and ("438"/$.ccls. or "257"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46

	L #	Hits	Search Text	DBs	Time Stamp
9	L9	12263	(((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips)) same (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)) same (encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
10	L10	59851	(grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) near8 (die or dice or IC or "integrated circuit" or chip or chips)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
11	L11	5948	((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) near8 (die or dice or IC or "integrated circuit" or chip or chips)) and ("438"/$.ccls. or "257"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
12	L12	11151	((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) near8 (die or dice or IC or "integrated circuit" or chip or chips)) near8 (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46

	L #	Hits	Search Text	DBs	Time Stamp
13	L13	1227	(((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) near8 (die or dice or IC or "integrated circuit" or chip or chips)) near8 (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)) and ("438"/$.ccls. or "257"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
14	L14	12263	(grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips) same (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6) same (encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
15	L15	2365	((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips) same (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6) same (encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic)) and ("438"/$.ccls. or "257"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46

	L #	Hits	Search Text	DBs	Time Stamp
16	L16	12109	((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) and (die or dice or IC or "integrated circuit" or chip or chips)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
17	L17	1231527	L1.ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
18	L18	24497	((encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic) and (die or dice or IC or "integrated circuit" or chip or chips)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
19	L19	28235	L1.ti. and ((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46

	L #	Hits	Search Text	DBs	Time Stamp
20	L20	1952	(((encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic) and (die or dice or IC or "integrated circuit" or chip or chips)).ti.) and ((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) same (die or dice or IC or "integrated circuit" or chip or chips))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:46
21	L22	2806	(438/106).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:53
22	L27	1696	(257/686).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:54
23	L28	725	(257/687).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 13:54

	L #	Hits	Search Text	DBs	Time Stamp
24	L29	2260	(257/712).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:03
25	L21	924	((((grease or greases or "animal fat" or oil$4 or wax$6 or solvent$4 or liquid$6 or fluid$4 or coolant$4) near8 (die or dice or IC or "integrated circuit" or chip or chips)) near8 (contain$4 or lid$3 or top$4 or cap$4 or cover$4 or enclosur$4 or cas$6 or cell$6)) and ("438"/$.ccls. or "257"/$.ccls.)) and (encapsulat$4 or resin$3 or thermoplastic$4 or epoxy or plastic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:14
26	L30	1165	(257/718).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:03
27	L31	10493	22 or 23 or 24 or 25 or 26 or 27 or 28 or 29 or 30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:13

	L #	Hits	Search Text	DBs	Time Stamp
28	L32	191	31 and 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:15
29	L33	111	32 and ((@ad<"19990831") or (@rlad<"19990831"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:15
30	L23	1046	(438/107).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:29
31	L34	26	(("6011304") or ("6215180") or ("5583378") or ("6175157") or ("6218202") or ("5907189") or ("5786631") or ("5930893") or ("5843810") or ("5834337") or ("5475040") or ("5910010") or ("5891755")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:31

	L #	Hits	Search Text	DBs	Time Stamp
32	L24	1163	(438/108).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:38
33	L25	497	(438/112).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 14:48
34	L26	520	(257/685).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/21 15:07

US-PAT-NO: 6359335

DOCUMENT-IDENTIFIER: US 6359335 B1
See image for Certificate of Correction

TITLE: Method of manufacturing a plurality of semiconductor packages and the resulting semiconductor package structures

---------- KWIC ---------

Brief Summary Text - BSTX (2):
The present invention relates generally to a method of encapsulating a semiconductor package assembly or an array of such semiconductor package assemblies typically arranged on a supporting panel, while protecting the package's exposed terminals.

Brief Summary Text - BSTX (4):
In the construction of semiconductor chip package assemblies, it has been found desirable to interpose encapsulating material between and/or around elements of the semiconductor packages in an effort to reduce and/or redistribute the strain and stress on the connectors between the semiconductor chip and a supporting circuitized substrate during operation of the chip, and to seal the elements against corrosion, as well as to insure intimate contact between the encapsulant, the semiconductor die and the other elements of the chip package.

Brief Summary Text - BSTX (7):
In some arrangements used heretofore, the compliant layer is formed by stenciling a thermoset resin onto the chip carrier and then curing the resin. Next, additional resin is applied to the exposed surface of the cured layer, this additional resin is partially cured, and the resulting tacky adhesive surface was used to bond the elastomeric layer to the chip and the

outside the periphery of the chip. The substrate terminals and the chip contacts are then electrically connected to one another by flexible, electrically conductive lead. A unitary support structure is then aligned with the chips and attached to or abutted against the compliant layer around the periphery of the chips. A curable liquid encapsulant is then deposited around at least a portion of the periphery of each chip on top the unitary support structure so as to encapsulate the leads and at least one surface of the chip. Alternately, the curable liquid encapsulant may deposited around at least a portion of the periphery of each chip so as to encapsulate the leads and at least one surface of the chip and the unitary support structure may then aligned with the chips and attached to (and/or embedded in) the encapsulant around the periphery of the chips. The unitary support structure may be conductive (electrically or thermally) or insulative and further may have apertures or slots therein for reducing voids or bubbles between the unitary support structure and the encapsulant during the attached step. Optionally, a additional step of applying uniform pressure to the chip assemblies prior to the curing step may be employed such that such pressure reduces voids or bubbles between the unitary support structure and the encapsulant. The encapsulant is then cured to define an integrated composite of chip packages which may be singulated into individual chip packages or into multi-chip modules. Typically, the substrate is held taut of a frame during the packaging process.

Brief Summary Text - BSTX (18):

FIG. 1 is a side cross-sectional view, illustrating a semiconductor chip package assembly being encapsulated in an inverted position within a frame, according to the present invention.

Brief Summary Text - BSTX (20):
FIGS. 3A and 3B show various views of the encapsulation technique shown in FIG. 1 used with a plurality of devices on a common frame, according to the present invention.

Brief Summary Text - BSTX (24):
FIGS. 6A-6G show the process steps for encapsulating a center bonded semiconductor chip package assembly, according to the present invention.

Brief Summary Text - BSTX (25):
FIGS. 7A-7G show the process steps for encapsulating a center bonded semiconductor chip package assembly as shown in FIGS. 6A-6G with a flexible membrane attached thereto, according to the present invention.

Brief Summary Text - BSTX (27):
FIGS. 9A-9D show the process steps for encapsulating a semiconductor chip package assembly in which the chip carrier is encapsulated leaving only the raised terminals to protrude from the face surface of the chip package, according to the present invention.

Brief Summary Text - BSTX (28):
FIGS. 10A-10D show a process similar to that shown in FIGS. 9A-9D except that the raised terminals are removed after the encapsulation/cure steps, according to the present invention.

Detailed Description Text - DETX (5):
Once the semiconductor chip assembly 10 has been positioned and attached to the coverlay and ring, encapsulation material 40 is introduced into the open area between the frame 42 and the periphery of the semiconductor chip assembly 10. The encapsulation material 40 is comprised of a curable liquid which will allow the leads 22 to "flex" after the encapsulant 40 has been cured in response to thermal cycling forces during operation of the finished package. In the preferred embodiment, the encapsulant is comprised of an

electronic
grade silicone-based or epoxy-based resin; although, other materials may be
used. The curing mechanism of the encapsulation material 40 will depend on the
particular encapsulant material used so that the encapsulant can be cured or
partially cured. Typical curing mechanisms are radiant energy, thermal energy,
moisture or ultraviolet light.

Detailed Description Text - DETX (7):
The semiconductor chip package assembly and frame/encapsulant surrounding
structure may then be attached to a PWB using a suitable conductive bonding
material, such as eutectic solder. Alternately, a dicing means (such as a
dicing saw, water jet, ultrasonic knife, rotary razor, laser, etc.) may be
employed to separate the encapsulated chip assembly structure from the frame 42
so that the resultant chip package is no wider or only slightly wider than the
periphery of the chip 12 itself. This allows for the operation of having a
protective "bumper" 44 of cured encapsulant material around the periphery of
the semiconductor chip assembly as shown in FIG. 2. In such an embodiment, the
dielectric layer 16 is juxtaposed with the contact bearing surface of the chip
12, as before; however, the dielectric layer 16 in the diced package embodiment
shown in FIG. 2 is larger than the contact bearing surface of the chip 12 such
that it extends beyond the perimeter of the chip 12. The encapsulant 40
correspondingly extends beyond the chip perimeter to form a bumper 44 of
encapsulant material. The bumper 44 further protects the edges of the chip and
the metallurgy of the joint between the leads 22 and the contacts 24. The
bumper also provides added durability to the package by protecting the sides of
the chip 12.

Detailed Description Text - DETX (9):
In an alternate embodiment shown in FIGS. 3A and 3B, the

encapsulant can be dispensed so that it just covers the cavity between the leads 22, the compliant layer 20 and the dielectric layer 16 such that the cured encapsulant either is deposited to approximately the level of the contact bearing surface of the chip 12 or just protrudes slightly from the cavity between the chip 12 and the coverlay 30. In such an embodiment, the encapsulated chip assembly is typically diced so that the finished package is no larger than the periphery of the chip 12 itself, as shown in FIGS. 4A and 4B.

Detailed Description Text - DETX (10):

The embodiment shown in FIGS. 3A and 3B show that the encapsulation of the semiconductor chip assemblies 10 can be performed on a plurality of package assemblies 10 simultaneously, i.e. where the aperture in the frame 42 is large enough to accept many semiconductor chip assemblies 10 on the same coverlay 30. In this embodiment, it is preferable to have each chip 12 connected to the same chip carrier 14/coverlay 30 combination, as shown in FIG. 3A. Added manufacturing efficiency can be reached by encapsulating a plurality of such packages within the same frame by dispensing encapsulant in a first direction between and along the adjacent packages from one side of the frame 42 to the next before having to dispense in an orthogonal direction between and along such packages. The encapsulated chip assemblies may then be cut away of "diced" into individual chip packages or into interconnected multi-chip packages. The encapsulation of many chips 12 simultaneously is preferred to facilitate the mass production of finished packages. As described above, the encapsulant 40 is deposited from the chip side of the coverlay 30 and the coverlay ensures that the encapsulant 40 is bounded when it is deposited in liquid form such that it does not escape through possible bonding apertures 50 (FIG. 4B) and contaminate the terminals 26 and thus impede any